Microbumping technology for Hybrid IR detectors, 10µm pitch and beyond

B. Majeed, P. Soussan, P. Le Boterf[1], P. Bouillon[1]
Imec
Kapeldreef 75, Leuven 3001, Belgium
[1]Sofradir, 364, route de valence, 38113 Veurey Voroize -France
Bivragh.majeed@imec.be

Abstract

In order to assess the feasibility of a more mass-manufacturable process, IMEC has developed microbump technologies down to 10µm pitch. The micro bumps are based on Cu/Ni/Sn semi additive plating and built at wafer level using a process fully compatible with standard packaging infrastructures.

Different test materials with 15, 10 and even 5µm pitch Sn microbumps were processed for a total amount of 640 X 512 (VGA), 1024 X 768 (XGA) and 3072 X 3072 pixels respectively.

The microbumped Si chips were assembled with glass chips, InGaAs and HgCdTe compounds and subjected to thermocycling reliability evaluation.

Introduction

Hybrid detectors rely on the heterogeneous integration of Si and other materials, since the manufacturing constraints and intrinsic performances of the materials are not compatible, especially in the infrared domain. In order to achieve a higher spatial resolution, the number of pixel needs to be increased while being limited by the vertical interconnect pitch density between the focal plane and the Si read out chip underneath. Such devices usually rely on Indium based bumps, involving lift-off processes that inherently limit the interconnect density and poses manufacturing challenges for large bump arrays.

The main challenge upon assembly is to avoid shortcuts between the bumps, while at the same time provide enough compliance to obtain proper yield of the interconnects. Our bumps consist of Cu, a Ni barrier layer and Sn finish. It was reported earlier that is CuSn bumps can have electromigration (EM) lifetimes similar to greater than eutectic PbSn bumps [1,2]. For smaller pitches below 15µm, seed removal becomes challenging as well due to higher undercut with wet processes. There have been studies to reduce the underetch including study by Hess with using ion beam etching processing, however the process suffered from an incoherent tin layer with a crown formation around the top surface [3]. In another approach reported by Yu [4], electroless Ni/Au is plated on already formed Al bumps to reduce the undercut. However, the use of gold in standard CMOS process flow/Fab is not an option. Also they reported use of dry etch for removal of Ta seed layer. It has been reported below 15µm pitch it is not possible to use wet etch processes due to high undercut. In this paper we report on the process with reduced undercut and no bump delamination down to 10µm pitch.

On the reliability side, we evaluate the reliability of the Sn based microbumps under cryogenics conditions . Sn being a candidate for the replacement of Indium currently widely used for such applications.

Fabrication details

The processing scheme involves formation of two bumps fabricated at imec 200mm Fab. The first peripherical bumps raws are there to facicilitate the underfill flip chip process. These bumps are approximately 1-3µm depending on the bump pitch and thickness. The schematic of the process flow is shown in figure 1. The process start with a dielectric and TiW/Cu seed layer. In our process, we have used two different approaches for metal 1 bump. In first case, a thick resist is spin coated and patterned. Metal 1 bump are then electroplated. In second case, a thick layer of Al is deposited. Al is then etched to form the bumps. For finer pitches later process was used due to restriction of total bump height. While with the use of first process, the same seed layer can be used for formation of metal 2 bumps. A thick 7µm resist is spin coated and patterned. Metal 2 bump are electroplated in Nexx stratus tool. The bump stack is Cu/Ni/Sn its total thickness varies as a function of bump pitch. After the plating the resist is stripped and seed etch is done. First a wet copper etchant is used to remove the Cu seed followed by wet etch to remove the TiW seed.

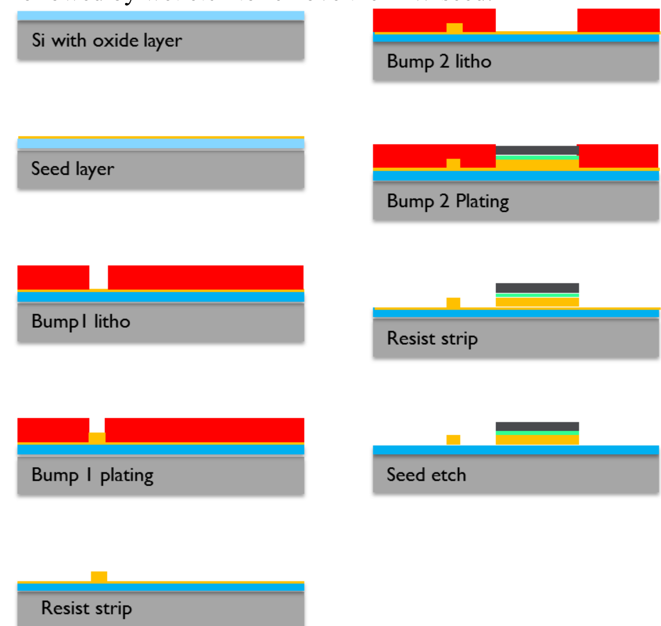

Figure1: Schematic process flow

Results

For 15µm pitch for metal 1 bump plating approach was used and same seed was used for metal 2 bumps. We investigated different thickness of Cu seed layer in order to reduce the underetch during seed etch., too thin film gave non uniform

978-1-4799-6994-4/14/$31.00 ©2014 IEEE

bump height while thickest film gave a large under etch. The optimal thickness was used for processes reported in this paper. Figure 1 shows the grapgh of thickness for different seed thickness. The measuremnts were done with high resolution surface profilometer across the wafer for eight points. For thinner seed shown in dashed line the variation in bump thickness is much larger.

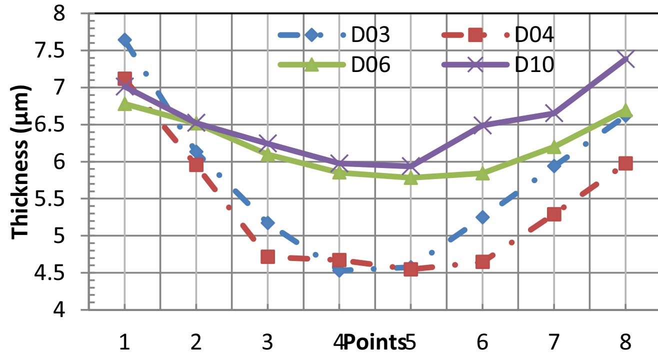

Figure2: Bump height for different seed thickness.

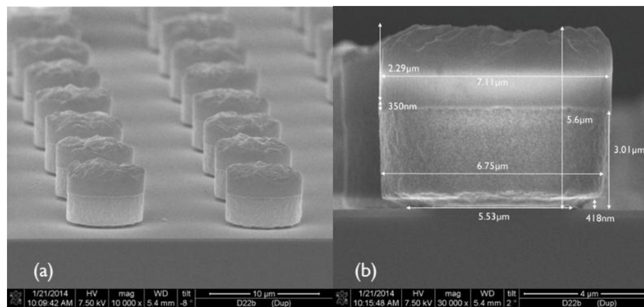

Figure 3a: A XSEM image showing the 15µm pitch bump array prior to assembly, (3b): A zoom image of single bumps with Cu/Ni/Sn and some underetch of Cu but no delamination of bumps

For 10µm bump similar process was used as pitch 15 and figure 4 shows the bump after fabrication. In this case, we did observe the underetch of the bump but still not very significant.

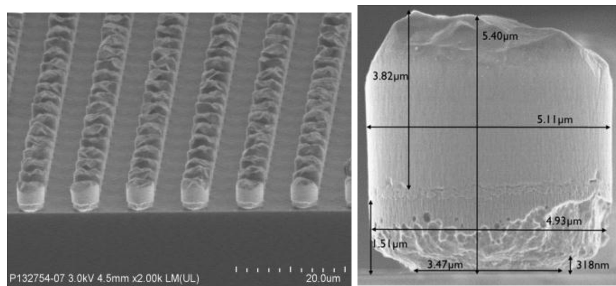

Figure 4a: A XSEM image showing the 10µm pitch bump array prior to assembly, (3b): A zoom image of single bumps with Cu/Ni/Sn and some underetch of Cu but no delamination of bumps

Later the 10µm pitch bumping process was modified.The metal1 posts were placed by Al patterned by dry etching. After the Al etch, a new seed of TiW and copper was deposited. The process was applied to a 200mm CMOS wafer for electrical purpose. Figure 5 shows the full wafer after bumping while figure 6 shows a representative bump.

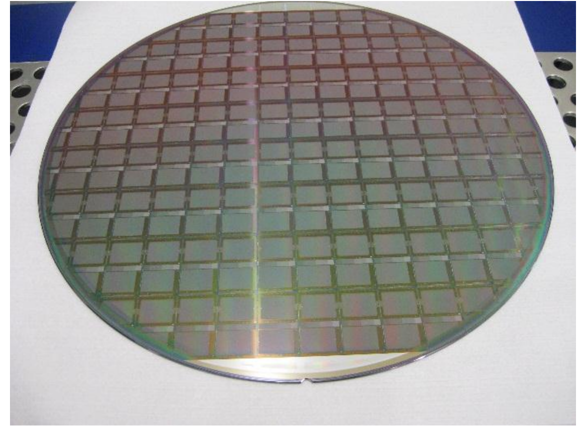

Figure5 : An optical images of a full device wafer with 10µm bump pitch

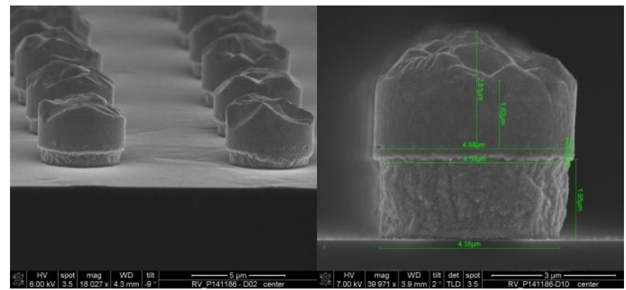

Figure 6: 10 µm pitch DC wafers bumps

Finally the microbumping technology was further evaluated for 5µm pitch microbump technology, well beyond the state of the art paving the way to multi million pixels technologies.

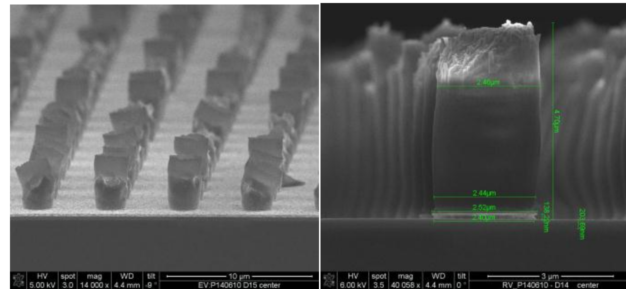

Figure 7: 5µm pitch bumps showing very little underetchs

Heterogeneous flip-chip development and results

The assembly of the sample was performed in a SET FC150 precision bonder which allowed a placement within +/- 1 µm accuracy. In first instance, the flip chip parameters were evaluated with glass parts with a coefficient of thermal expansion matched to silicon. In addition, these glass parts were coated with UBM pads representative of the infra-red detection circuit for diode connection, as can be seen on figure 8.

For both 640 X 512 pitch 15 µm and 1024 X 768 pitch 10 µm samples, design of experiments have been applied in order

to determine the major parameters involved in the bonding process.

Figure 8 shows the schematic of the process bonding process. The diameter of the UBM is slightly larger than the bump.

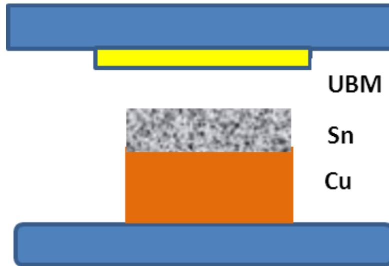

Figure 8: Schematic of the bonding process.

Among the different factors analyzed, the following are the most significant for bonding:

- Diameter of the Cu/Sn µbump
- Pressure applied during thermo-compression
- Temperature applied during thermo-compression

range	640 X 512 pitch 15 µm	1024 X 768 pitch 10 µm
µbump diameter (µm)	6 µm to 8 µm	4 µm to 5 µm
Pressure (N)	50N to 700 N	50N to 700 N
Temperature of thermo-compression (°C)	180°c to 250°C	180°c to 250°C

Table1: range of thermo-compression parameters for the design of experiments

This led us to optimum conditions to realize the Infra-red substrate hybridization.

Figure 9 and 10 shows a FIB cross-section of bonded samples on glass substrate for 15 and 10µm pitch bumps respectively. Its shows very good alignment and formation of Cu/Sn intermetallic and no squeeze out or shorts to the adjacent bump. For 10µm bump a larger UBM bump is used but still no squeeze out is observed as shown in figure10.

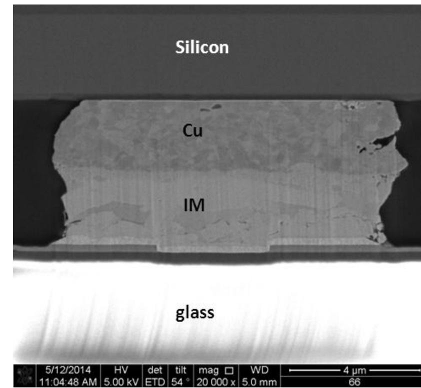

Figure 9: FIB X-section image of a bump of a 15 µm pitch bonded sample

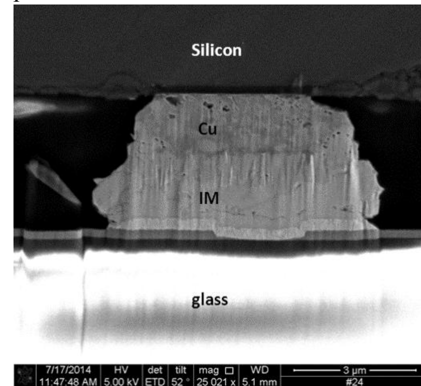

Figure 10 : FIB X-section image of a bump of a 10 µm pitch bonded sample

Shear testing and SAM characterization on Glass Chips

In order to measure the yield of connection on the glass part, shear testing was performed. Initially, in the absence of daisy chain structure, the analysis of the bonded µbumps was carried out through optical microscope inspection. The observation is being facilitated by the presence of very reflective pads on the glass substrate increasing the contrast, as can be seen on figure 11. This characterization was possible as long as the bonded parts did not undergo an underfill process.

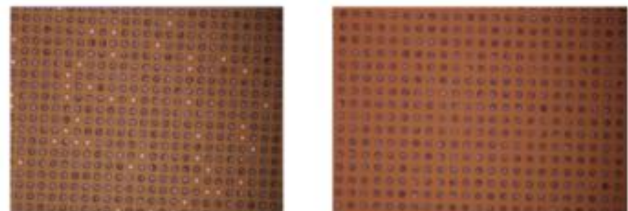

Figure 11: Optical image of a 10µm pitch shear test before and after bonding optimization. pads are visible when not connected.

After bonding optimization, we achieve a yield close to 100% for both formats according to this optical characterization. The repeatability was checked on more than 5 bonding's for each format.

The capillary underfill process was successfully developed using the glass samples on 15 and 10 µm pitch. Later on, a Scanning Acoustic Microscopy was performed on the non-transparent substrates in order to check the connectivity and underfill uniformity. No void has been detected on any of the component.

640 X 512 pitch 15 µm InGaAs and HgCdTe bonding and testing

6 silicon chips with 640X512 format, at 15µm pitch Cu/Sn µbumps have been hybridized to InGaAs and HgCdTe infrared detection circuits. Once hybridized, the components have been dispatched for characterization and thermal cycling. InGaAs component do not operate under cryogenic temperature, therefore a cycling of -40°C/100°C was applied. HgCdTe components, which operate in cryogenic environment , were however thermo cycled in the range 80K/293K up to 1700 cycles.

On figure 12, we show a typical inspection by cross-section of the bonded sample. This type of inspection is used to assess the quality of the bonded sample before and after cycling. As can be seen on table2 , among the 6 components with structures close to 640X512 P15 Infra-red detectors, all presented a good interconnect yield before and after cycling.

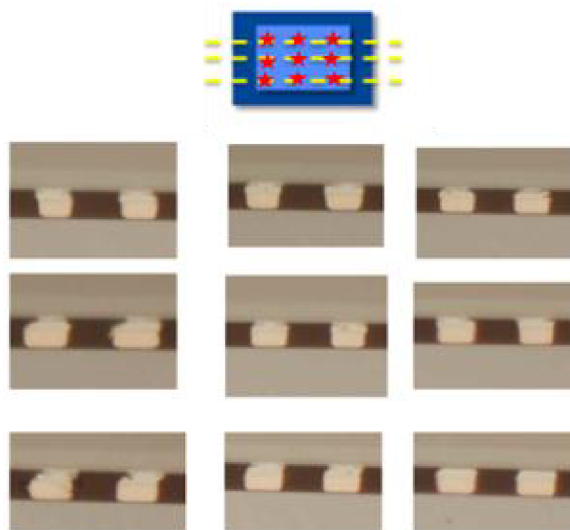

Figure 12: 9 zones microscopic inspection of a InGaAs cross section (no short or open detected along 3 lines)

component 640X512	detection circuit	SAM analysis	cross section analysis	cycling	cross section after cycling
1	InGaAs	OK	OK	-	-
2	InGaAs	OK	-	100X -40°c/100°C	OK
3	HgCdTe	OK	OK	-	-
4	HgCdTe	OK	OK	-	-
5	HgCdTe	OK		1700X 80K/293K	OK
6	HgCdTe	OK		1700X 80K/293K	OK

Table 2: Assembly and reliability evaluation of InGaAs and HgCdTe 640X512 15µm pitch samples

1024 X 768 pitch 10 µm HgCdTe bonding and testing

The methodology used for hybridization characterization was the same as the 15 µm pitch. 8 components have been flip chipped. The first one was tested and proved the interconnect quality (no detection of short or open). Three samples went directly to cross section analysis whereas four went to cryo cycling (80K-293K), up to 960 cycles.

Among the 8 components, only one had an interconnect issue, as displayed on figure 13. On this specific one, at least 50% of the µbumps did not connect the detection circuit and a strong misalignment was observed. The presence of a particle during thermo-compression cycle was suspected. The remaining 7 components had a interconnect yield of 100 % and a misalignment below 2 µm. .

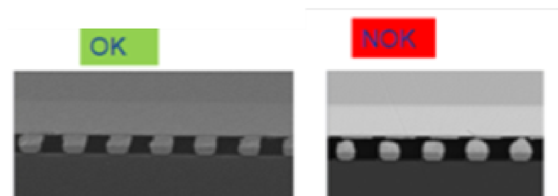

Figure 13: Microscopic inspection of interconnect bonding. The right sample presented a strong misalignment.

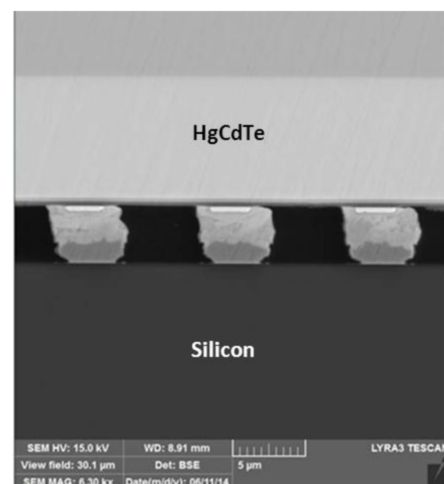

Figure 14: SEM picture of a 10µm pitch cross section after 960X cycles 80K-293K

As can be seen on table 3 below, all samples that were properly bonded have survived cryo testing.

component 1024X768 P10	shear test	SAM analysis	cross section analysis	Cryo cycling X960 + cross section
1	OK	-		
2	-	OK	OK	
3	-	OK	OK	
4	-	NOK	NOK	
5	-	OK		OK
6	-	OK		OK
7	-	OK		OK
8	-	OK		OK

Table 3: Assembly and reliability evaluation of HgCdTe 1024X768 10µmpitch samples

Conclusions

200mm Si wafers were successfully bumped down to 10 µm pitch. We successfully hybridized the Cu/Ni/Sn microbumps to large array InGaAs and HgCdTe detection circuits. These components followed respectively thermal cycles (-40°C/100°C and 80K/293K) without any visible structural change. The compounds that were used are realistic vehicles, the assembly process was optimized through designs of experiments and the chips were successfully underfilled. The performance of the assembly was evaluated by SAM, shear test and cross sections.

We show that the Sn based microbump technology has the potential to be used for heterogeneous integration of HgCdTe detection circuits onto Si ROIC, operating in extreme cryogenic conditions, moving down to 5µm pitch

Work Perspectives

- A more complete 1024 X 768 pixels format with 10µm pitch CuSn Daisy chain will help us to push the electrical characterization for this type of structure.
- We propose to evaluate the technology to the 5 µm pitch with a 3072 X 3072 pixels format in a second time

Acknowledgments

The authors would like to thanks help from NCI team with XSEM and Fab for help with the processing.

References

1. S. L. Wright, R. Polastre, H. Gan, L. P. Buchwalter, R. Horton, P. S. Andry, E. Sprogis, C. Patel, C. Tsang, J. Knickerbocker, J. R. Lloyd, A. Sharma and M. S. Sti-Jayantha, "Characterization of Micro-bump C4 interconnects for Si-Carrier SOP applications," 55th Electronic Components and Technology
2. K.N. Tu , Hsiang-Yao Hsiao, ", Chih Chen bTransition from flip chip solder joint to 3D IC microbump: Its effect on microstructure anisotropy", Microelectronics Reliability 53 (2013) 2–6
3. J Hess and H Vogt, "Sacrificial ion beam etching process for seed layer removal of 6 µm pitch CuSn micro bumps", Materials Science and Engineering, 41 (2012) 012005.
4. Aibin Yu, John H Lau, Soon Wee Ho, Aditya Kumar, Wai Yin Hnin, Da-Quan Yu, Ming Ching Jong, Vaidyanathan Kripesh, Damaruganath Pinjala, Dim-Lee Kwong"Study of 15µm Pitch Solder Microbumps for 3D IC Integration", *Proc 59th Electronic Components and Technology Conf*, San Diego,CA, May. 2009, pp.6-10