Die-to-Die and Die-to-Wafer Bonding solution for High Density, Fine Pitch Micro-Bumped Die

Gilbert Lecarpentier*, Joeri De Vos**

** SET S.A.S. (Smart Equipment Technology), 131 Impasse Barteudet, 74490 Saint Jeoire, France*

** IMEC, Kapeldreef 75, Leuven B-3001, Belgium

OUTLINE

- Introduction
- Placement schemes and Bonding schemes
- Die-to-Die Bonding
  - Demonstrator
  - Bonding Process
  - Results
- Summary

GLOBAL ROAD MAP FOR 3D-INTEGRATION WITH TSV

YOLE DÉVELOPPEMENT

Qualification

First product on the market!

~ 1 year

Logic + Memory "wide I/O interfaces"

CPU / GPU

Mem

Logic

TSI

eDRAM

Logic 22-28nm

high perf. ASICs

HPC

Logic multi-cores

Baseband / APE

Mobile appliances

Wide IO mem

BB / APE

DRAM

Logic

Digital & Analog partitioned "3D-SOCs"

Large die

Logic only interposers

Logic

N+1

N+2

N+3

Small die

ASICs

Logic N

Logic N+2

Analog / RF

Heterogeneous 3DICs

eFlash

eDRAM

Logic

RF

MEMS

Analog

HB-LED interposer modules

LED

Silicon Module

LED

Driver

Multi-chip modules

LED

LED

Driver

Stacked Memories

Stacked DDR3

≥ 1.6Ghz

≥ 16Gbit

Stacked NAND Flash / NVM

Power, RF, Analog & Mixed signals components

Ground TSV

PA / IGBT / MOSFET

RF-SiP

IPD

Power GaN

Sapphire or Silicon

MEMS & Sensors

Sensor

MEMS

ASIC

3D interposer

ASIC

MEMS

Interposer

MEMS cavity

MEMS

Cap

Opto WLP

Sensor

Glass vias

MOEMS

Multi-ASIC

CMOS / MEMS

ASIC

Analog/RF

CMOS imagers

ShellOP "Edge"

SOC CIS

TSV / WLP

SOC CIS

WL Optics

SOC CIS

Consumer BSI

SOC CIS 1.1µm

High-end BSI

CIS

ISP + mem

CIS

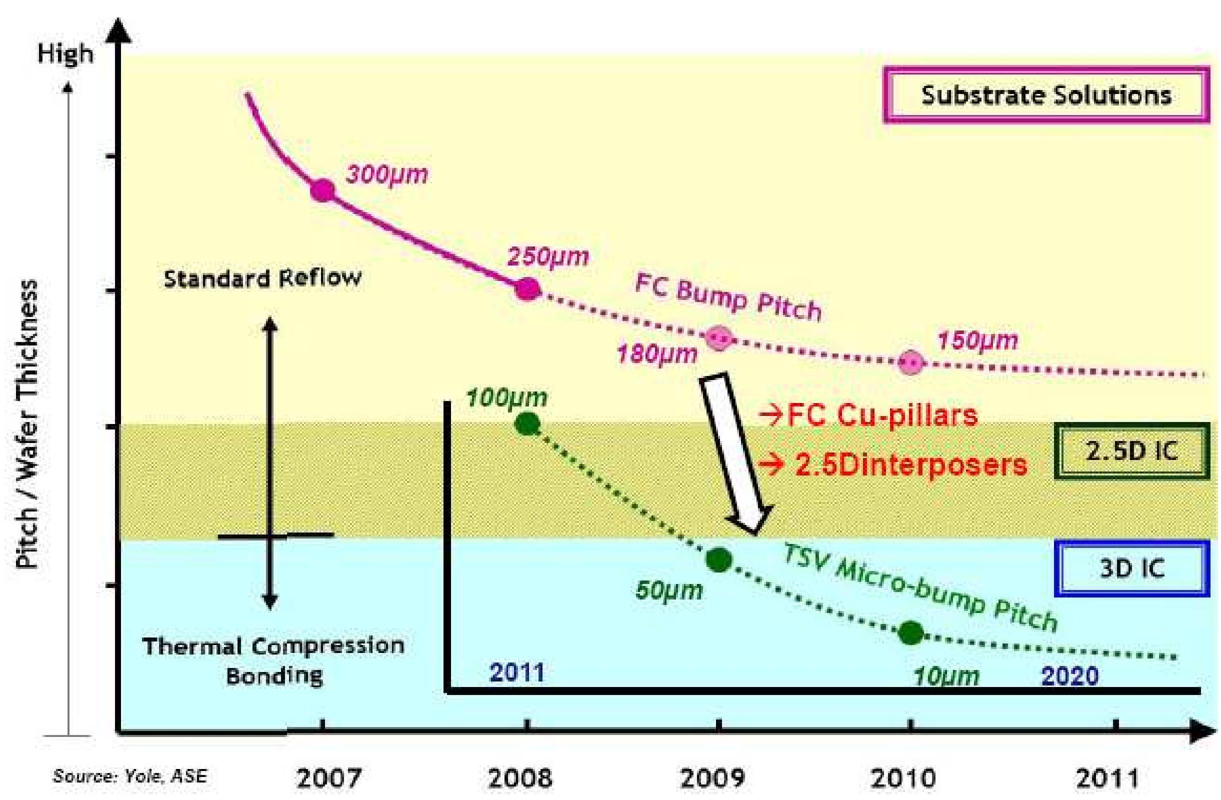
DSP

mem

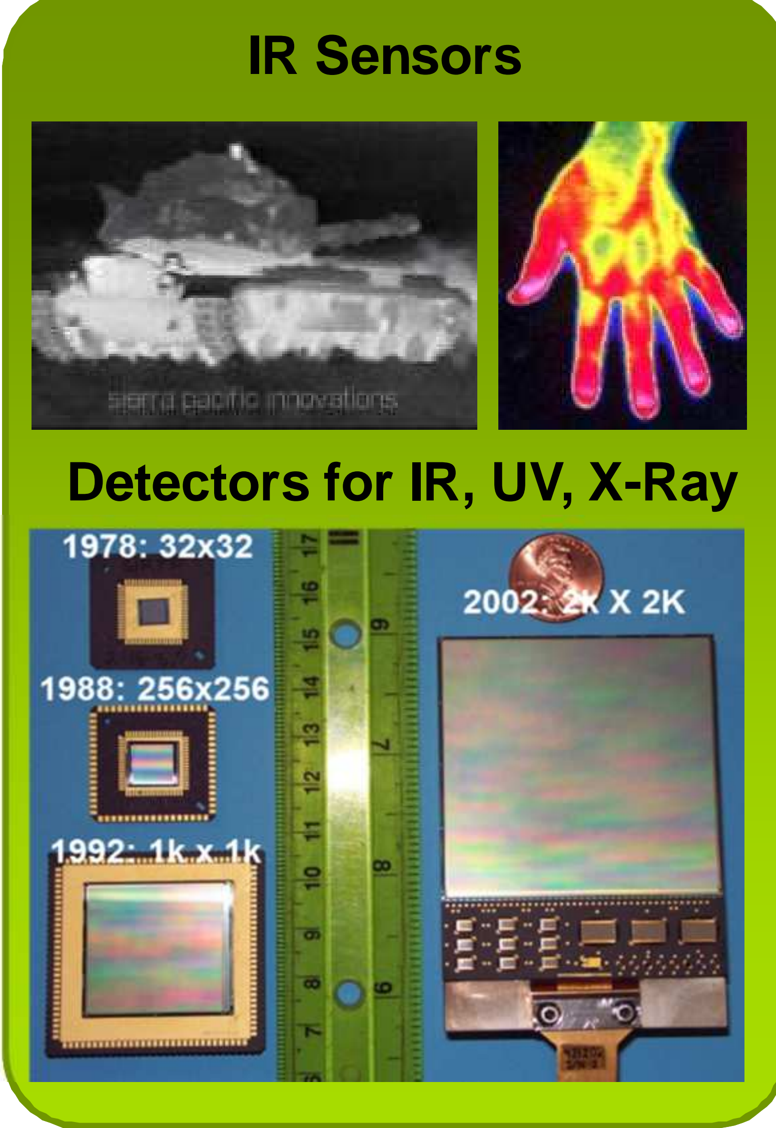
2006 | 2007 | 2008 | 2009 | 2010 | 2011 | 2012 | 2013 | 2014 | 2015 | 2016

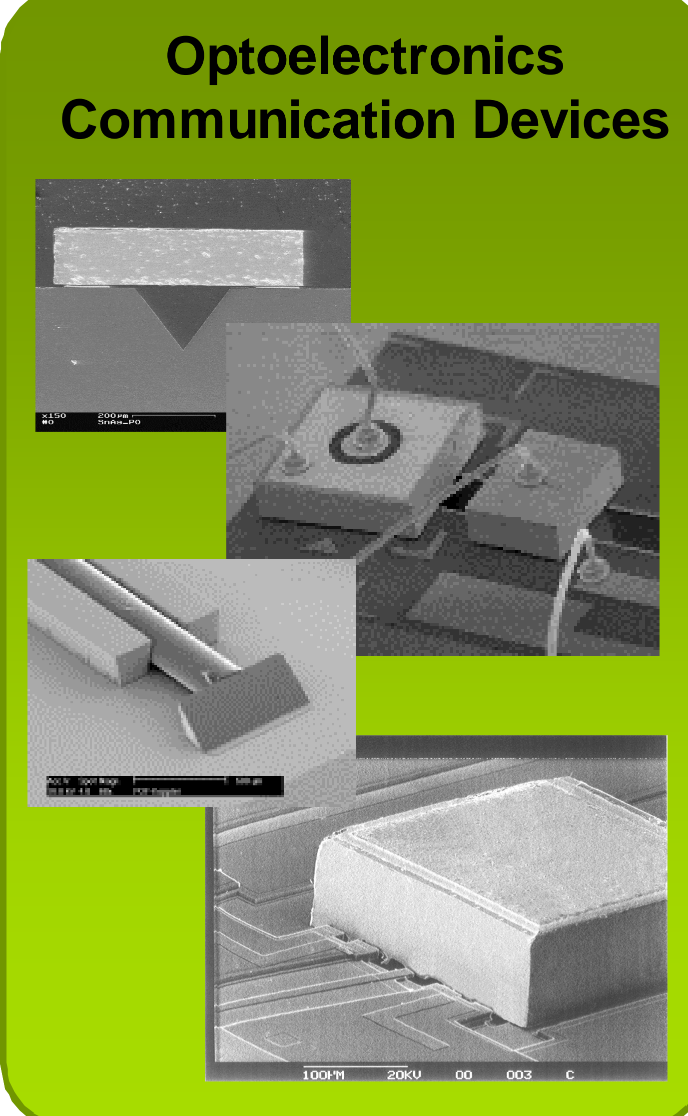
ASSEMBLY TRANSITION ROADMAP IMPACT ON EQUIPMENT DESIGN

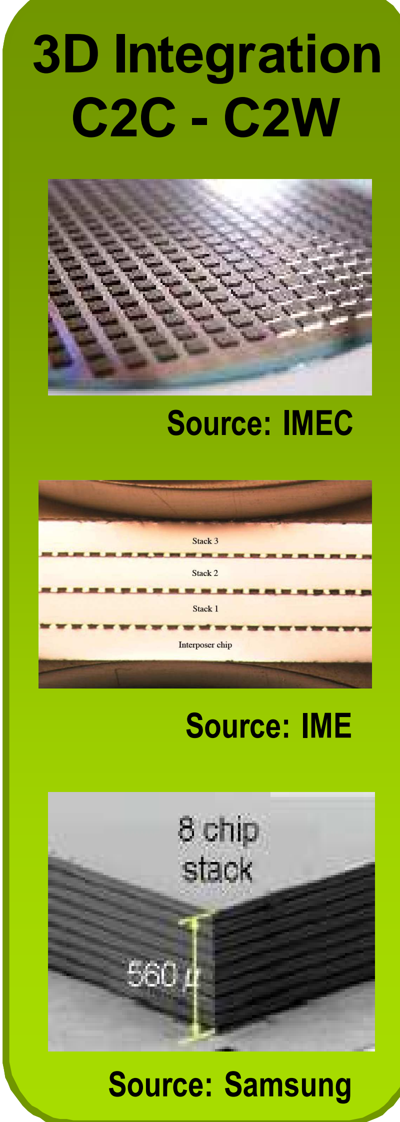
- **Road map shows a migration towards Thermocompression bonding rather than reflow bonding**
  - → **Tougher requirements on bonding equipment**
  - → **Force Increases while pitch and Bump Size decrease**



DIE TO DIE / DIE TO SUBSTRATE / DIE TO WAFER
APPLICATIONS REQUIRING HIGH ACCURACY PLACEMENT







PLACEMENT AND BONDING SCHEMES

ALIGNMENT

- Face-to-Face / Flip Chip (F2F)
- Face-to-Back (F2B)

PLACEMENT

- Die-to-Die (D2D / C2C)
- Die-to-Wafer Bonding (D2W / C2W)

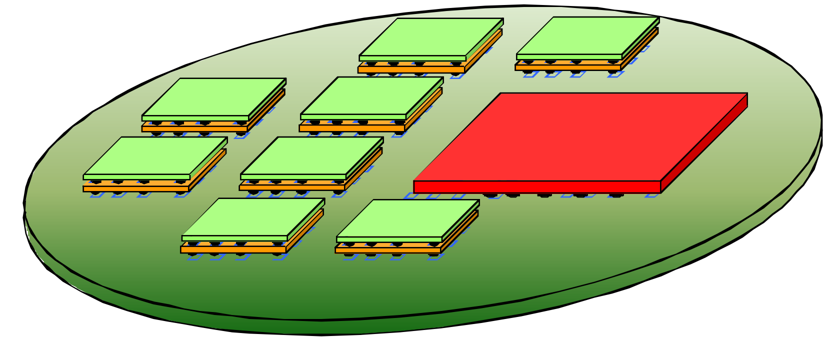
BONDING

- In situ Bonding
  - In-Situ Reflow
  - Thermocompression
- Sequential placement followed by gang bonding

DIE-TO-WAFER (D2W) PLACEMENT

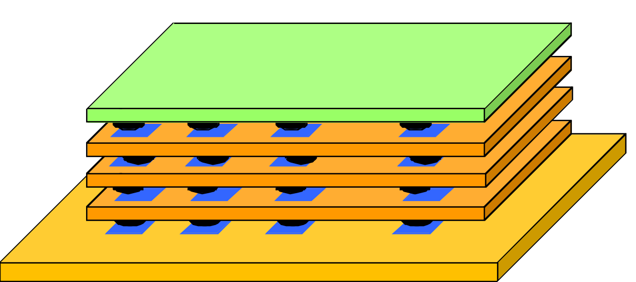
- ☹ Throughput
  - Single Chip Placement
- ☺ High Yield
  - Known Good Die
  - Good Overlay
- ☺ Flexibility

  \- Component and wafer sizes
- ☺ **Heterogeneity !**
  - Different Technologies
  - Different suppliers, …



DIE TO DIE (D2D) BONDING / DIE STACKING

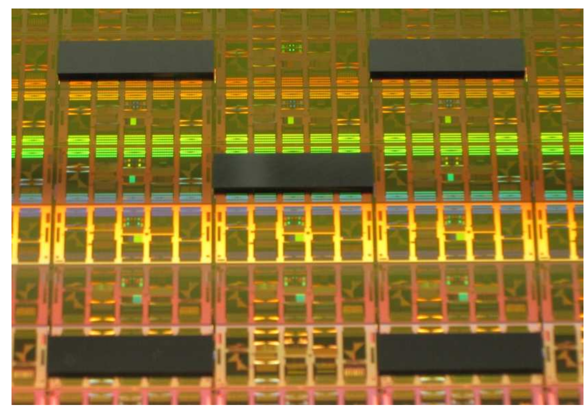
- 😐 Throughput
  - Single Chip Placement
  - Multiple Alignment stage capable
- ☺ High Yield
  - Known Good Die
  - Good Overlay
- 😐 Flexibility
  - Component sizes (?)
- ☺ **Heterogeneity !**
  - Different Technologies
  - Different suppliers, …



CHIP PLACEMENT

Face-to-Face / Flip Chip (F2F)

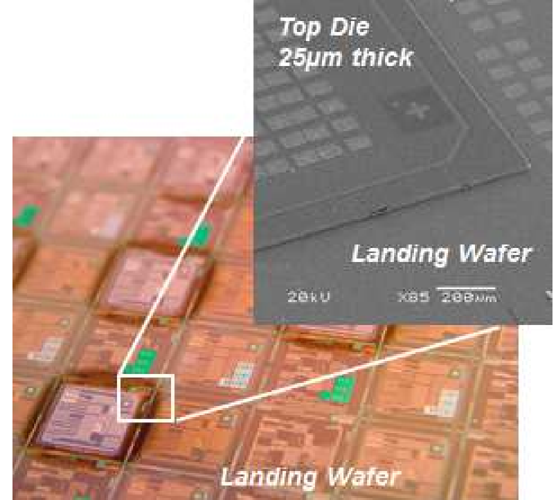
- Chip must be flipped after pick up prior to being transferred to the bond head
- Alignment can be made by Inter-Component optics literally at bonding position providing high accuracy placement capability
- Post bonding testing is difficult



Source: SEMATECH

Face-to-Back (F2B)

- Chip can be placed directly after pick up, blind alignment with memorized information is performed
- For higher accuracy, alignment can still be made by Inter-Component optics in case the via offer good enough image



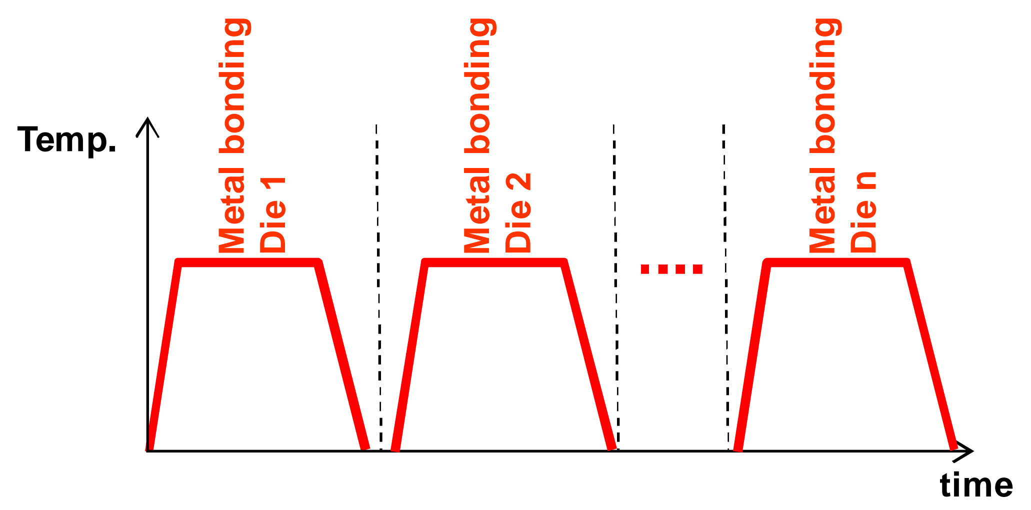
Source: IMEC

set
Smart Equipment Technology

DIE-TO-WAFER BONDING
IN-SITU Vs COLLECTIVE, TEMPERATURE PROFILE

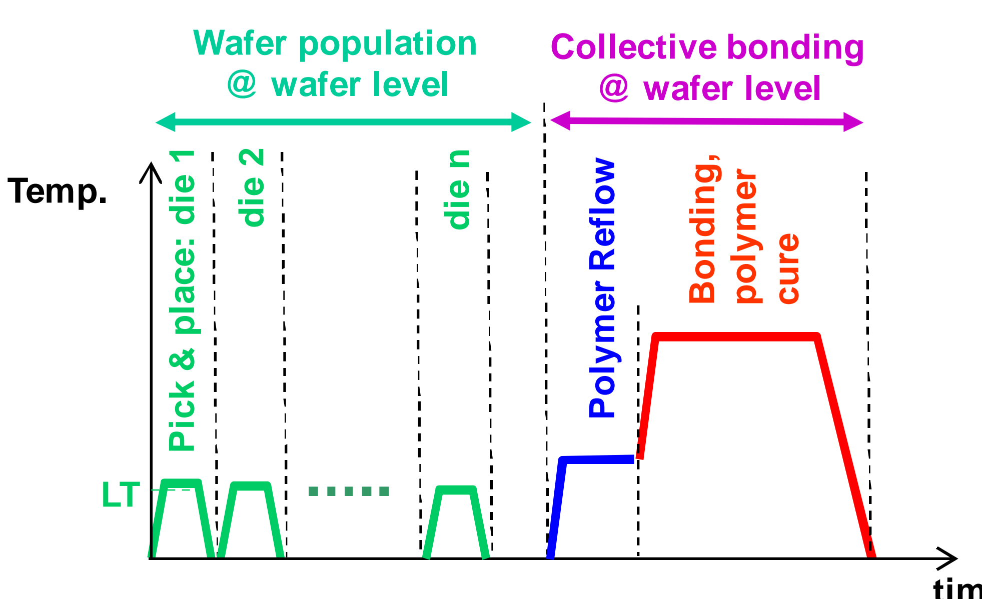
Sequential D2W bonding

- ☺ High Accuracy capability, controlled by the bonder
- ☹ Time consuming
- ☹ Landing wafer sees several bonding T-cycles



Collective D2W bonding

- ☺ Time efficiency
- ☺ Landing wafer sees only one temperature cycle
- ☹ Accuracy depends upon pre-attachment method and global bonder



DIE-TO-DIE BONDING DEMONSTRATOR: HYBRID IMAGER

High density 20µm pitch
Applications: FPGA, Fully hybrid imagers

Detector

ROIC

PCB

DIE-TO-DIE BONDING DEMONSTRATOR μBUMP FULL AREA ARRAY

- Bump diameter: 10μm
- Pitch: 20μm
- Designed to investigate very high bump yield
- Face-to-Face assembly
- 440 long daisy chains of 1766 bumps each

	Top die	Landing die
Die size	20.2 x 18.7 mm thickness 725 μm	21.4 x 21.4 mm thickness 725 μm
# bumps	~ 1000 x 925 bumps	

DIE-TO-DIE BONDING DEMONSTRATOR MODULE WITH LONG DAISY CHAIN ARRAY

Long daisy chains

short daisy chains/ test structures

Bond pad area

BOTTOM DIE

M1 → M44

Top die

Bottom die

1 2 3 4 5

R1 R2

S1 S2 S3 S23

S4

1 module

R: NORMAL CHAIN RESISTANCE
S: TO CHECK SHORTS

44 modules (M1 to M44) / die
per module: 5 x 2 interwoven daisy chains of 1766 bumps
→ 440 daisy chains in total / die
Length 1daisy chain: about 5cm.

set
Smart Equipment Technology

DIE-TO-DIE BONDING DEMONSTRATOR
µBUMP -- CuSn (Cu Pillar)

Si
Top die
Cu
10µm
Bond pad
Bumps
Sn
Cu
Al
0µm
Si_3N_4
SiO_2
Si
Landing die

Cu

Sn
Cu

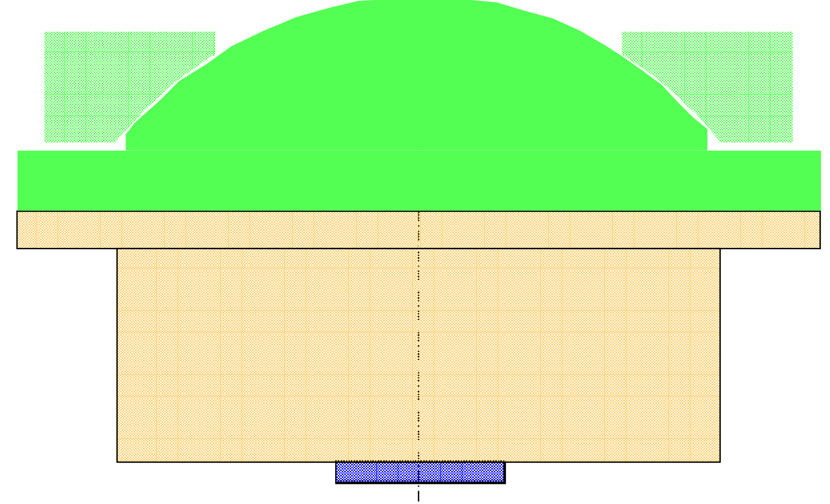
D2D Face-to-Face flip chip assembly done at 250℃, 3min, 5MPa
No under fill used to assess stacking yield of µbumps only

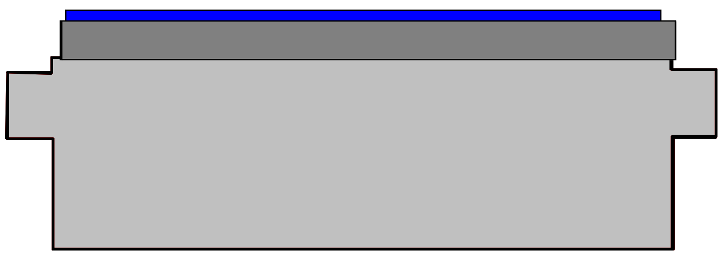
DIE-TO-DIE BONDING / EXPERIMENTAL SET UP

- Die to Die Alignment, Placement & Bonding was performed on the SET-FC150
- Flexible High Accuracy Die / Flip Chip Bonder
- ± 1 µm Post Bond Accuracy

ALIGNMENT AND PLACEMENT SEQUENCE

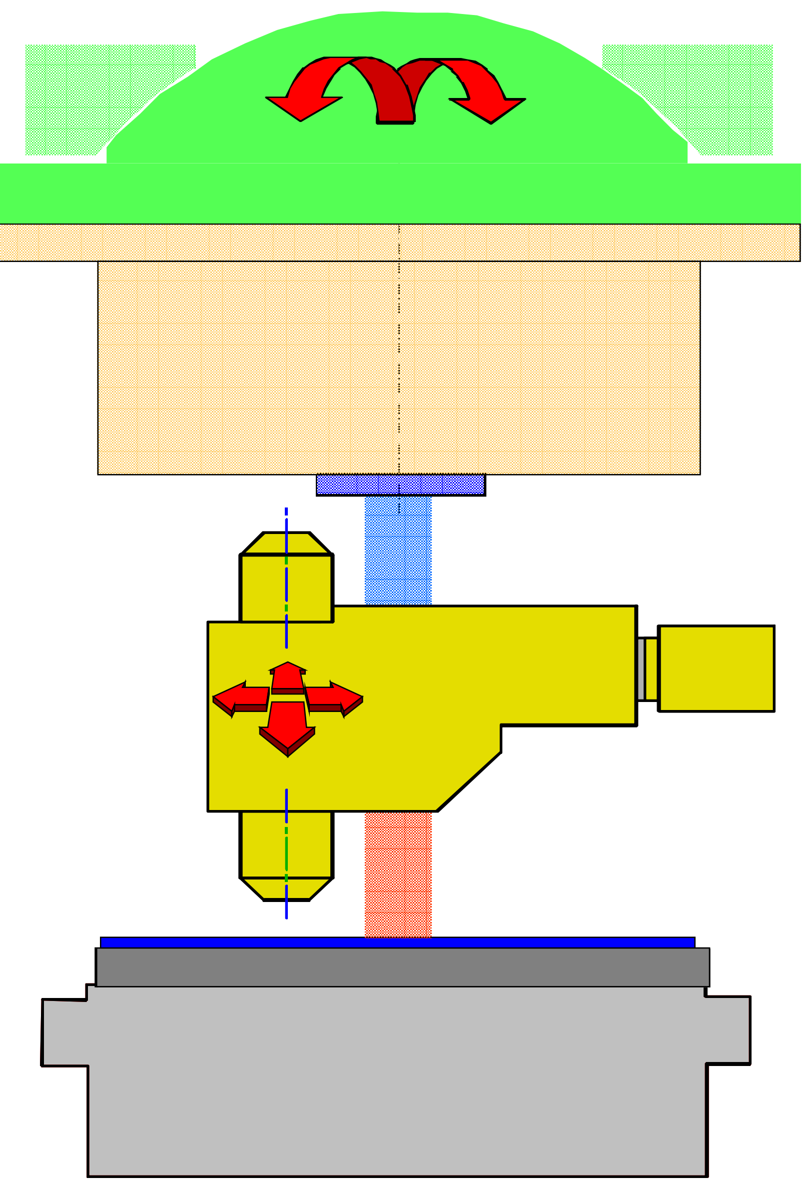
- Die is vacuum-secured on a Silicon Carbide Pick Up tool





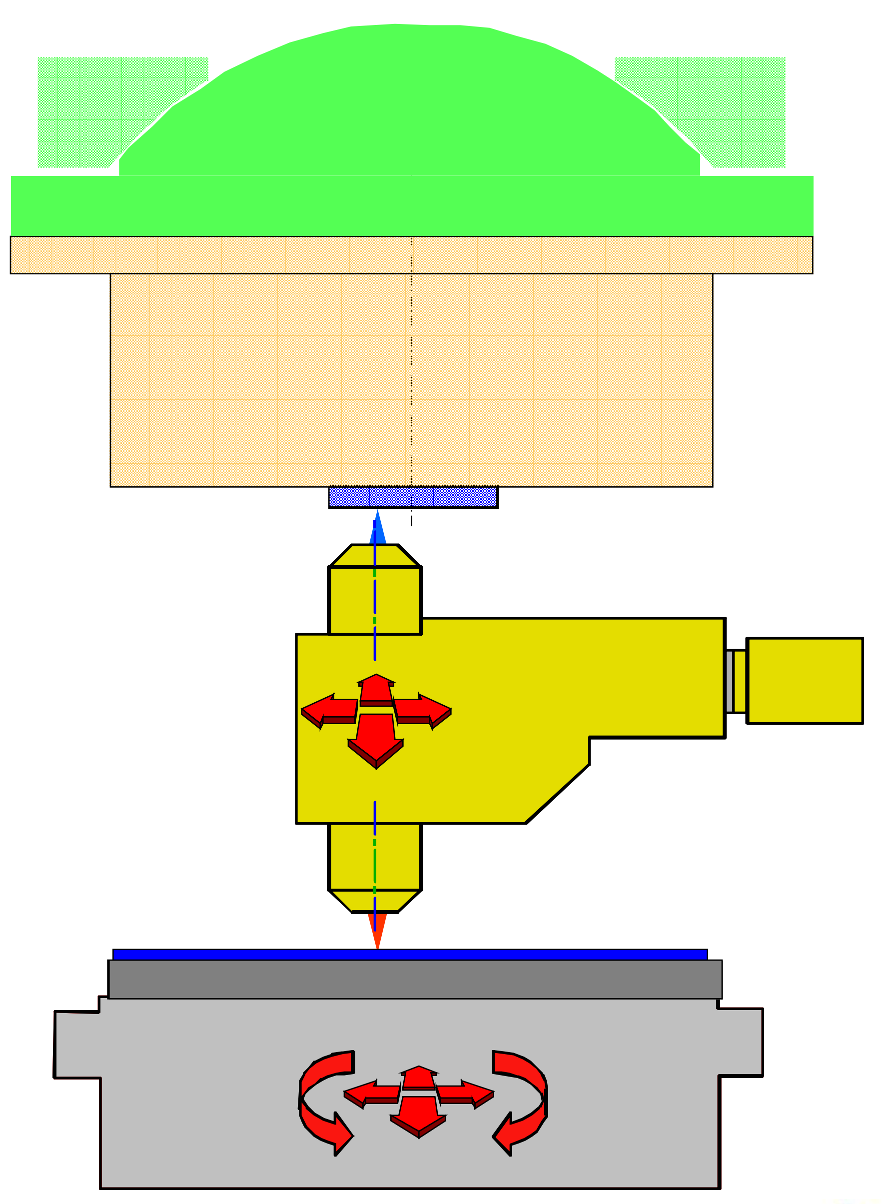
ALIGNMENT AND PLACEMENT SEQUENCE

- Die is vacuum-secured on a Silicon Carbide Pick Up tool
- Parallelism can be actively adjusted by motorized sphere coupled with an autocollimator



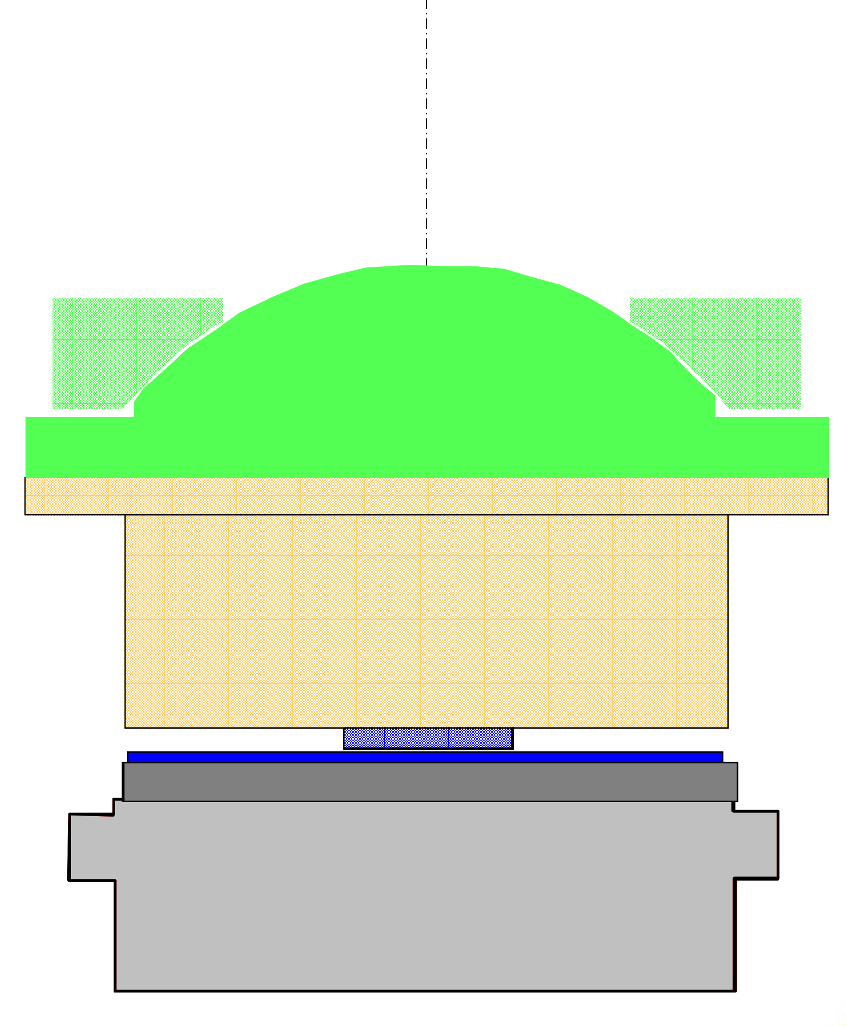
ALIGNMENT AND PLACEMENT SEQUENCE

- Die is vacuum-secured on a Silicon Carbide Pick Up tool
- Parallelism can be actively adjusted by motorized sphere coupled with an autocollimator
- XYθ Alignment is achieved by inserted microscope between the die and the wafer



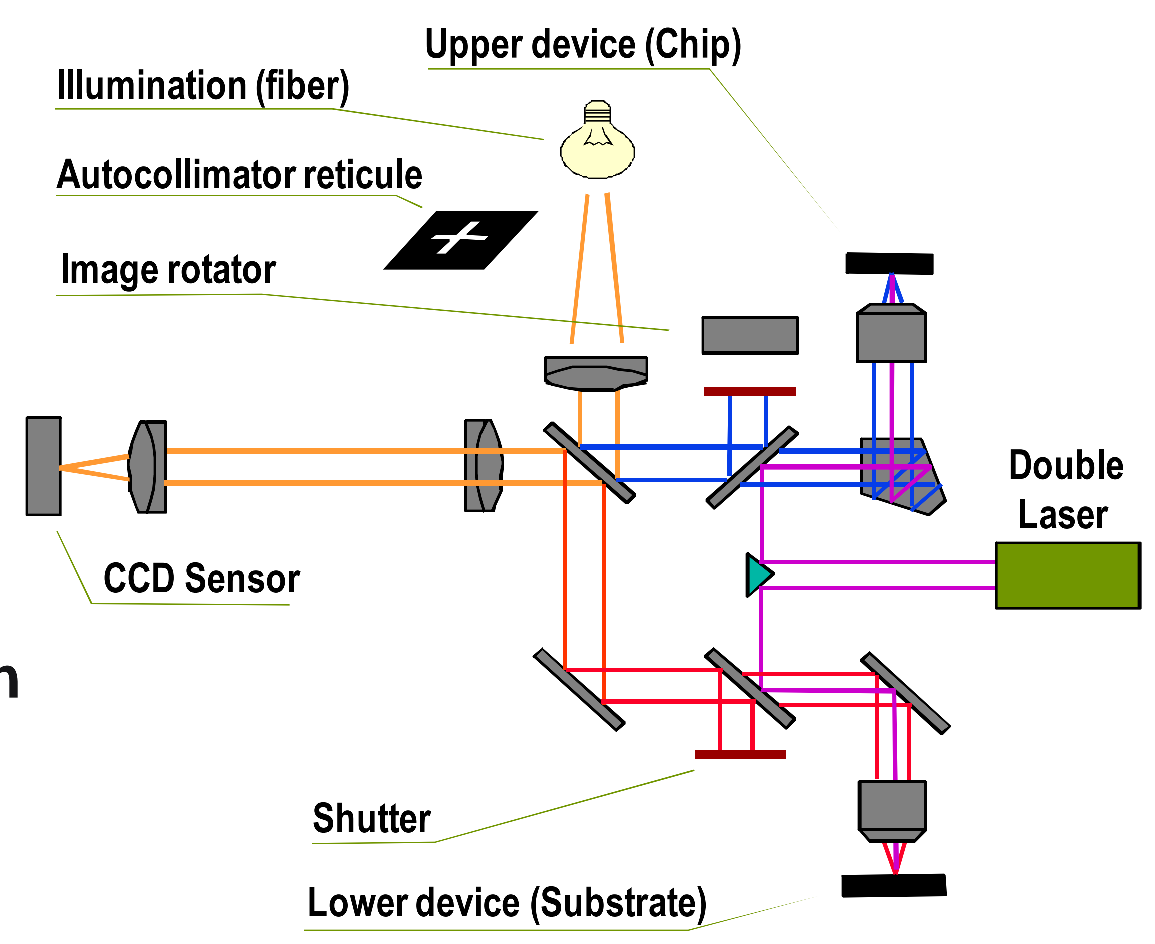
ALIGNMENT AND PLACEMENT SEQUENCE

- Die is vacuum-secured on a Silicon Carbide Pick Up tool
- Parallelism can be actively adjusted by motorized sphere coupled with an autocollimator
- XYθ Alignment is achieved by inserted microscope between the die and the wafer
- Bond Head moves down to search contact and Place/bond die on wafer

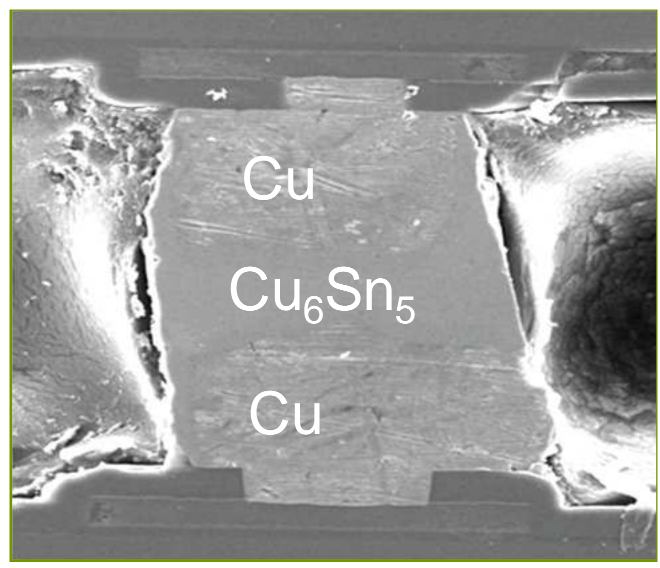


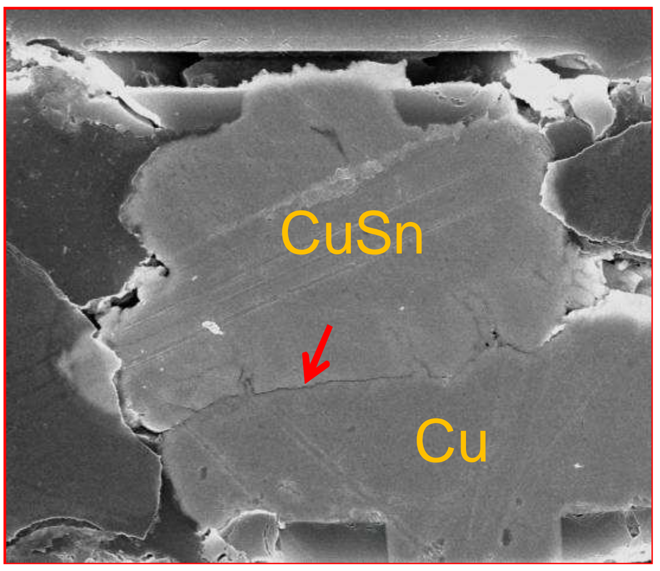
ALIGNMENT SEQUENCE
PARALLELISM WITH ADVANCED LASER LEVELING

- **Supplement to auto-collimator, for components with:**
  - Low Reflectivity
  - Bowed or Warped
  - < 2 mm
- **Laser focus based design**
  - Focuses at 3 to 8 points, then calculates leveling
  - Automated operation



DIE-TO-DIE BONDING DEMONSTRATOR
BONDING RESULTS





- **Copper Cleaning Step**
- **Process of Record**

Temperature elevated after dice are placed in proximity to enable confinement

→ Good bond is achieved
→ Bump resistance 58mΩ

- **No Copper Cleaning Step**
- **Process of Record**

→ No contact (open circuit)

DIE-TO-DIE BONDING DEMONSTRATOR
Mechanical characterization: shear strength testing

bump diameter: 7.5µm

- Shear tool width: 35µm
- Shear height: 1µm
- Shear distance : 50µm
- Shear velocity : 40µm/sec
- Touchdown velocity: 40µm/sec

Ti/Cu	TiW/Cu
Average: 0.385 grf	**Average: 0.452 grf**
	Increase of 6.7%
Std dev: 0.042 grf	**Std dev: 0.055 grf**

DEMONSTRATOR - DAISY CHAIN YIELD
fixed conditions Cu bump

100%
90%
80%
70%
60%
50%
40%
30%
20%
10%
0%

D82 D83 D84 D85 D86 D87 D88 D89 D90 D91 D92 D93

Type	Cu	CuSn	Cu	CuSn	Cu	CuSn	Cu	CuSn
Cu seed etch	A	B	A	B	A	B	A	B
TiW etch	POR	POR	POR	POR	POR	OE	POR	OE
Cu Clean	YES	NO	YES	YES	YES	YES	YES	NO

OE= 30% over etch time

Daisy chain yield 2PP-measurement on 440 daisy chains with 1766 bumps

Very high daisy chain yield

- Functional
- Open
- Short

<u>CuSn bump DOE</u>

No yield influence when

- ↗ TiW OE time by 30%
- Adding Cu clean

set
Smart Equipment Technology

DIE-TO-DIE BONDING DEMONSTRATOR BONDING RESULTS SUMMARY

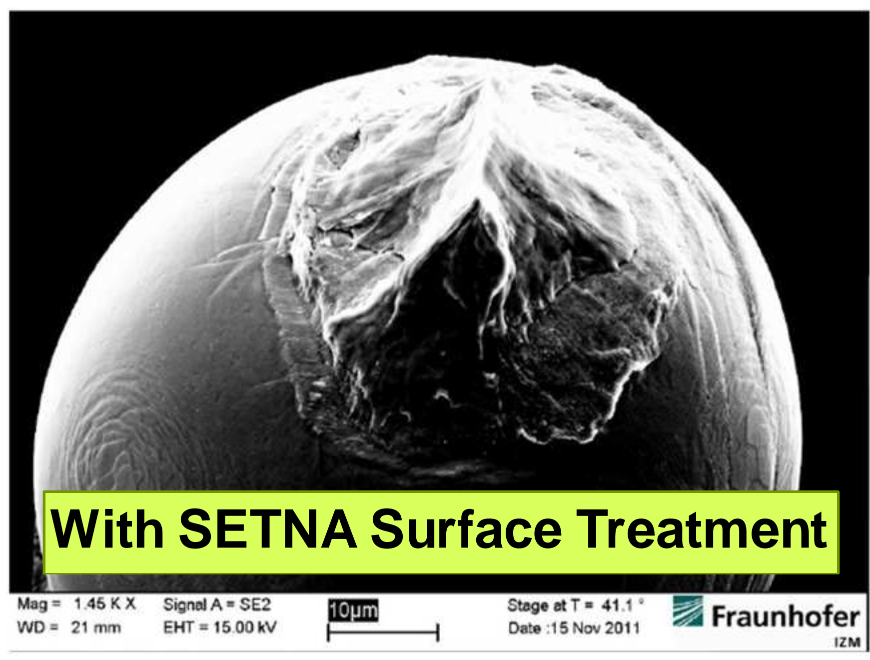
- **Processing scheme 20µm pitch CuSn bumping for 3D stacking**
  - POR = TiW/Cu seed, seed ethant B for both bumps;
    Cu clean on Cu bump
  - No yielding daisy chains for Cu bumps not treated with Cu clean
  - Time between Cu clean to assembly: 4 months → no time critical
  - No impact on daisy chain yield when TiW etch time is increased

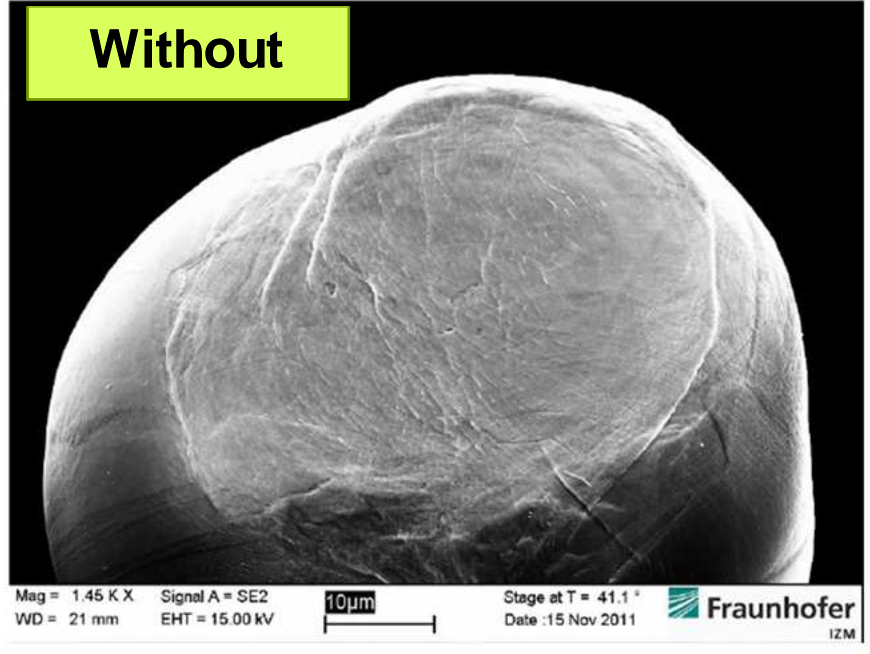
- **High yield numbers (87.5 ~ 99.5%) shown on large area 20 µm bump pitch daisy chains with 10 µm diameter CuSn bumps implies a defect density below 50 for 1 million bumps (< 50 ppm)**

COPPER CLEAN

IMEC has not disclosed their copper clean process

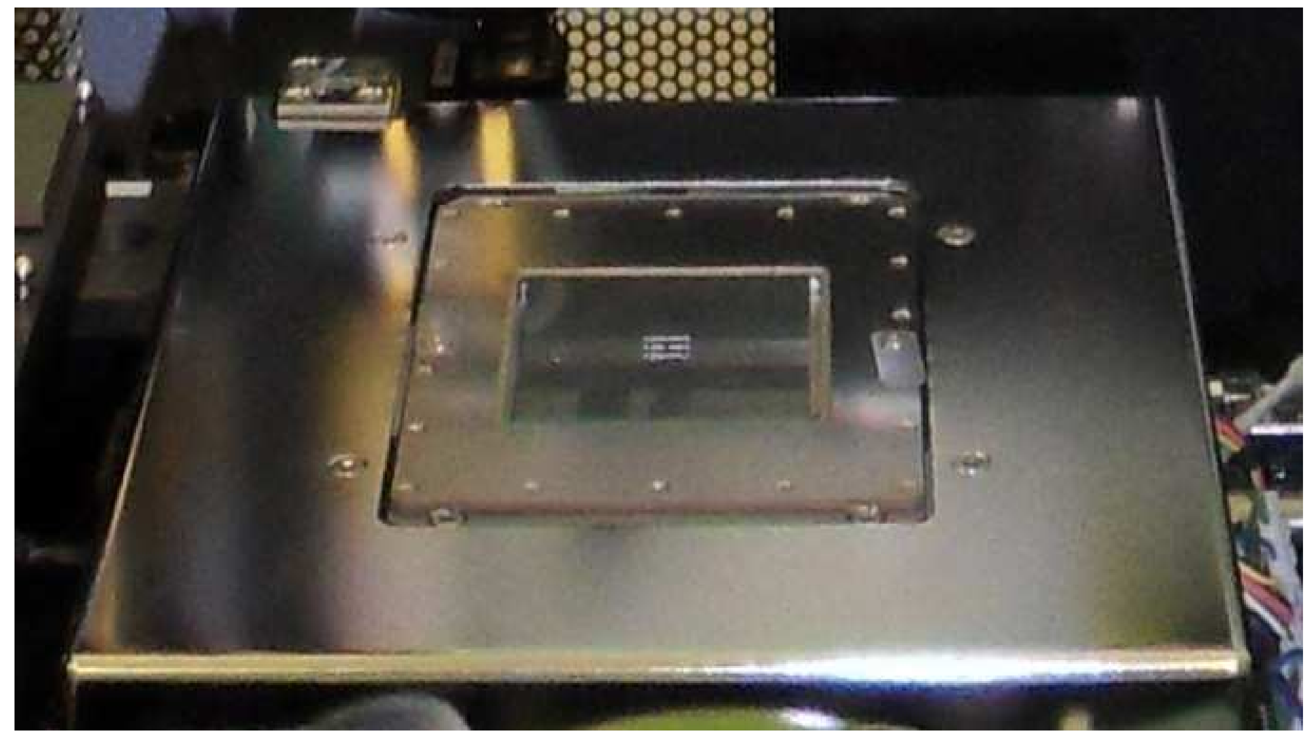
- **SETNA (SET distributor in North America) has developed its own surface preparation system *(Patent pending)***
- **It removes native oxide on various metals, and applies a thin passivation layer preventing re-oxidation even at elevated temperature**





DIE-TO-DIE BONDING DEMONSTRATOR
BONDING IN NEUTRAL GAS ENVIRONMENT

- Gas confinement made easier for Die-to-Die as bond head and substrate chuck have same or similar dimensions



DIE-TO-DIE BONDING DEMONSTRATOR
BONDING IN NEUTRAL GAS ENVIRONMENT

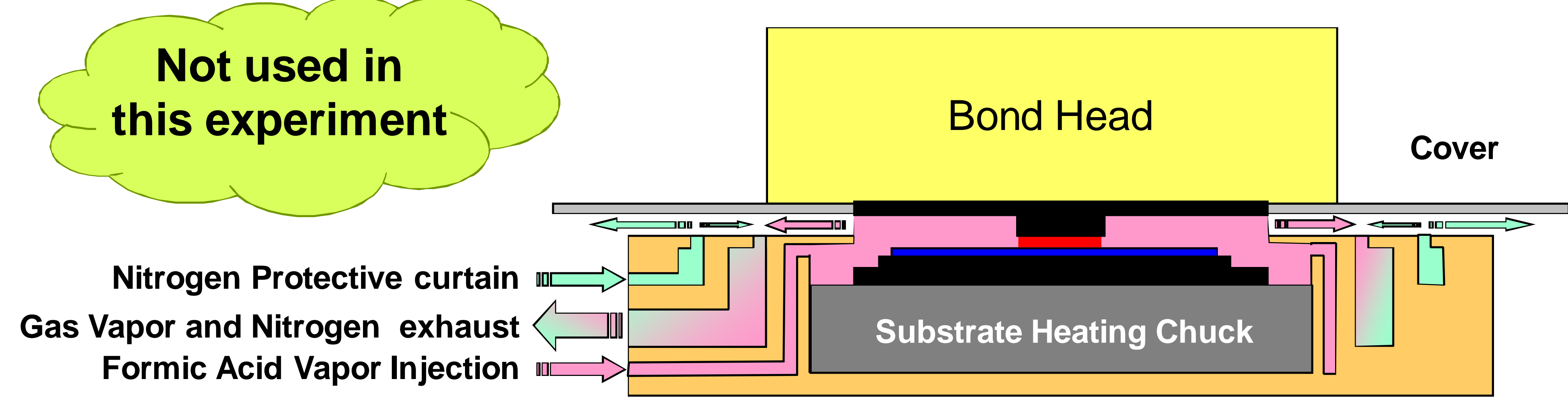
- Gas confinement made easier for Die-to-Die as bond head and substrate chuck have same or similar dimensions
- In case of small Bottom die (<20mm) a confinement cover can be used to reduce the window and ensure confinement efficiency even when bond head is not in bonding position

Confinement cover clamp

Confinement cover clamp

set
Smart Equipment Technology

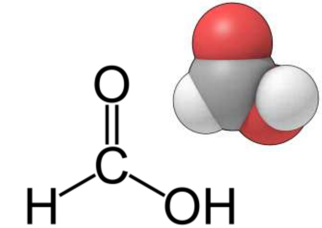
REMOVAL OF OXIDE PRIOR TO BONDING
IN-SITU CONFINEMENT CHAMBER (D2D VERSION)

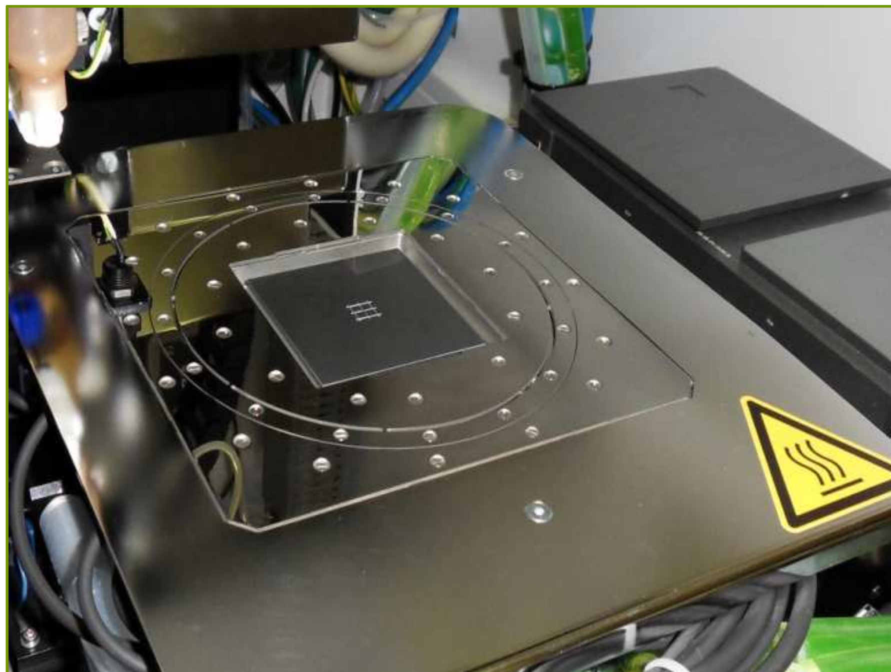


- The Semi-Open Confinement includes a Contactless Cover Plate attached to the Bond Head it becomes active only when components are in proximity
- Process Gas is injected towards the components (programmable gap)
- Exhaust Ring prevents process gas dissemination in the environment
- External Nitrogen curtain prevents Oxygen introduction in the Confinement Chamber

REMOVAL OF OXIDE PRIOR TO BONDING
REDUCTION CHAMBER HARDWARE

- **Photos of the D2D version of the micro-chamber**





View of Chuck

View of Bond Head

REMOVAL OF OXIDE PRIOR TO BONDING IN-SITU CONFINEMENT CHAMBER (D2W VERSION)

Formic Acid Vapor Injection
Gas Vapor and Nitrogen exhaust
Nitrogen Protective curtain

Bonding Arm

Chip Heating Chuck

Substrate heating chuck

- **In the Die-to-Wafer version of the Confinement Chamber, the chamber part is attached to the bond head, the contact less cover function is performed by the wafer itself**
- **This experimental set up has some challenges**
  - Local areas of the wafer see several gas reduction cycles
  - During wafer population, exposed areas oxidize

DEMONSTRATOR - HYBRID IMAGER
µBUMP ROADMAP

Source: imec

Pitch (µm)

160
140
120
100
80
60
40
20
0

2009
2010
2011
2012
2013
2014

Cu Pillar based Flip Chip
Cu-Sn based Micro Bump

100 µm
75 µm
40 µm
20 µm
10 µm

FINER PITCH IMPACT ON BONDING EQUIPMENT

Depending upon bonding process and bump material, post bond alignment requirement is

30 ~ 10% of bump size

(10µm pitch, 5µm Bump)

0,5µm Post Bond Alignment

- Higher Camera Resolution
- Better automatic vision system
- Higher machine stiffness and stability
- Higher Alignment Stage resolution
- Better thermal management

FC300R PILOT PRODUCTION EQUIPMENT AT 240 UPH

ALIGMENT WITH INTER-COMPONENT OPTICS / FC300R

- **Requires machine stiffness/stability and optics resolution adapted to the alignment accuracy target**
- **Alignment Accuracy at 3 sigma = 0,12 µm**

Automatic Alignment Accuracy

AlignErrorRX
AlignErrorRY

0,2
0,1
0
-0,1
-0,2

29/2/12 18:14
29/2/12 19:14
29/2/12 20:14
29/2/12 21:14
29/2/12 22:14
29/2/12 23:14
1/3/12 0:14
1/3/12 1:14
1/3/12 2:14
1/3/12 3:14
1/3/12 4:14
1/3/12 5:14
1/3/12 6:14
1/3/12 7:14

PLACEMENT AT ROOM TEMPERATURE / FC300R

- **Automatic Calibration check every hour**
- **Post Bond Accuracy at 3 sigma = 0,51 µm**

Placement Accuracy

X1 Y1 correction

0,5
0
-0,5

29/2/12 18:28
29/2/12 19:28
29/2/12 20:28
29/2/12 21:28
29/2/12 22:28
29/2/12 23:28
1/3/12 0:28
1/3/12 1:28
1/3/12 2:28
1/3/12 3:28
1/3/12 4:28

THERMOCOMPRESSION BONDING SIMULATION

- **Automatic Calibration check every hour**
- **Placement Accuracy at 3 sigma → X 0,45 µm, Y 0,65 µm (TC Bonding simulation at 300°C)**

Bond head 50mm / Substrate Chuck 50mm / TC Bonding simulation with Quartz Chips (12x12mm) -- Température 300 °C

0,5
0
-0,5

8/2/12 17:16
8/2/12 18:16
8/2/12 19:16
8/2/12 20:16
8/2/12 21:16
8/2/12 22:16
8/2/12 23:16
9/2/12 0:16
9/2/12 1:16
9/2/12 2:16
9/2/12 3:16
9/2/12 4:16
9/2/12 5:16
9/2/12 6:16
9/2/12 7:16
9/2/12 8:16
9/2/12 9:16

X1 Y1

SUMMARY

- Using the SET-FC150, high accuracy Flip Chip Bonder, Connecting full area µbump array on large 20mm die has been demonstrated using a Chip to Chip, Face to Face (Flip Chip) placement and Thermo Compression process
- Cleaning cupper pad/pillar is required to obtain good contact
- µbump roadmap showing bump pitch reduction to 10µm with eventually larger die induces tougher requirement on die parallelsim adjustment, alignment and post bond accuracy
- The new generation bonder FC300R achieves this requirement

Thank you for your attention
Questions ?

Die-to-Die and Die-to-Wafer Bonding solution for High Density, Fine Pitch Micro-Bumped Die

Gilbert Lecarpentier*, Joeri De Vos**

** SET S.A.S. (Smart Equipment Technology), 131 Impasse Barteudet, 74490 Saint Jeoire, France*

** IMEC, Kapeldreef 75, Leuven B-3001, Belgium